AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A process of manufacturing a semiconductor device, the process comprising: ~~the step of~~

forming elements on a wafer, and thereafter forming an interlayer insulating film on the wafer over at least the elements;

~~chemical mechanical polishing for~~ flattening [[an]]the interlayer insulating film ~~deposited on a wafer on which desired elements are in advance~~ formed by chemical mechanical polishing, and

wherein a stopper layer is formed [[on a]]only at an edge region of the device where otherwise the interlayer insulating film would be ~~which will be~~ excessively polished through the chemical mechanical polishing, wherein the stopper layer is formed before or after forming the interlayer insulating film.

2. (Currently amended) A process according to claim 1, wherein the stopper layer has a thickness greater than a ~~an intended~~ thickness of the interlayer insulating film to be obtained in the final product ~~after the polishing by a thickness of the interlayer insulating film reduced by the polishing~~.

3. (Original) A process according to claim 1 further comprising the step of photolithography for forming a connection hole in the interlayer insulating film, wherein the stopper layer has a width greater than that of a resist layer to be removed from a wafer periphery portion in the photolithography step.

4. (Currently amended) A process according to claim 1, wherein the stopper layer [[is a]]comprises silicon nitride[[film]].

5. (Currently amended) A process according to claim 1, wherein the interlayer insulating film [[is a]]comprises silicon oxide[[film]].

6. (Original) A process according to claim 3, wherein the width of the resist layer to be removed from the wafer periphery portion is 3-4 mm.

7. (Original) A process according to claim 1, wherein the stopper layer is removed after the chemical mechanical polishing.

8. (Currently amended) A process according to claim 2, wherein the stopper layer has a thickness greater than the ~~intended~~ thickness of the interlayer insulating film in the final product by 50-700 Å.

9. (New) A method of making a semiconductor device, the method comprising:

forming elements to be at least partially supported by a substrate,

forming a stopper layer so that the stopper layer is located at an edge portion of the device but not at any central portion of the device;

forming an interlayer insulating film over at least the elements and the stopper layer; and

chemical mechanical polishing the interlayer insulating film so as to remove the interlayer insulating film over the stopper layer, wherein a polishing rate of the interlayer insulating film is greater than a polishing rate of the stopper layer, so that the interlayer insulating film is not excessively polished at the edge portion of the device.

10. (New) A method of making a semiconductor device, the method comprising:

forming elements on a substrate,

forming an interlayer insulating film over at least the elements;

forming a stopper layer over only an edge portion of the interlayer insulating film so that the stopper layer is located at an edge portion of the device but not at any central portion of the device;

chemical mechanical polishing the interlayer insulating film and the stopper layer, wherein a polishing rate of the interlayer insulating film is greater than a polishing rate of the stopper layer, so that the interlayer insulating film is not excessively polished at the edge portion of the device; and

after the chemical mechanical polishing, removing the stopper layer from the edge portion of the interlayer insulating film so as to expose a portion of the interlayer insulating film that had previously been under the stopper layer.